CLAIMS

What is claimed is:

[Note: Bold and double-bracketed ***and size-reduced*** **cross-referencing text** (e.g., **[** [100] **]**) is provided in the below claims as an aid for readability and for finding corresponding (but not limiting) examples of support in the specification. The so-bracketed text is not intended to add any limitation whatsoever to the claims and should be deleted in legal interpretations of the claims and should also be deleted from the final published version of the claims.]

1. A method **[**[300]**]** of forming sidewall dielectric on an ONO-type memory cell stack **[**[310]**]** where at least one sidewall of the ONO-type memory cell stack includes a plurality of exposed material layers respectively composed of different materials, the method comprising:

(a) subjecting the at least one sidewall to a dry ISSG process (In-Situ Steam Generation) where the dry ISSG process comprises:

(a.1) flowing molecular oxygen (O_2) towards the stack; and

(a.2) flowing molecular hydrogen (H_2) towards the stack, where the volumetric flow ratio of the H_2 to the O_2 is less than about 0.2.

2. The sidewall dielectric forming method **[**[300]**]** of Claim 1 wherein:

(a.2a) said volumetric flow ratio of H_2/O_2 is less than about 0.1.

3. The sidewall dielectric forming method **[**[300]**]** of Claim 1 wherein:

(a.2a) said volumetric flow ratio of H_2/O_2 is equal to, or less than, about 0.02.

4. The sidewall dielectric forming method **[**[300]**]** of Claim 1 and further comprising:

(b) rapidly heating the flowing oxygen (O_2) and flowing hydrogen (H_2)

to a temperature in the range of about 850°C to about 1050°C as they flow towards said at least one sidewall.

5. The sidewall dielectric forming method [[300]] of Claim 1 and further comprising:

(b) continuing the subjecting of the at least one sidewall to the dry ISSG process for a duration selected from the range of about 20 seconds to about 300 seconds.

6. The sidewall dielectric forming method [[300]] of Claim 1 and further comprising:

(a.1a) setting or varying the O_2 flow rate over the range of about 3slm to about 10slm (ten standard liters per minute).

7. The sidewall dielectric forming method [[300]] of Claim 1 and further comprising:

(a.2a) setting or varying the H_2 flow rate over the range of about 0.1slm to about 1slm.

8. The sidewall dielectric forming method [[300]] of Claim 1 and further comprising:

(b) establishing a chamber pressure for the flowing oxygen (O_2) and flowing hydrogen (H_2) in the range of about 5 Torr to about 50 Torr.

9. The sidewall dielectric forming method [[300]] of Claim 1 and further wherein:

(b) said plurality of exposed material layers of the ONO-type memory cell stack includes:

(b.1) a first silicon nitride layer [[315]] ;

(b.2) a first silicon layer [[318]]; and

(b.3) a first silicon oxide layer [[316]] .

10. The sidewall dielectric forming method [[300]] of Claim 9 and further wherein said plurality of exposed material layers of the ONO-type memory cell stack includes:

(b.4) a second silicon layer [[312]];

(b.5) a second silicon oxide layer [[314]];

(b.6) a tunnel dielectric layer [[311]] ;

(b.7) wherein the first silicon nitride layer [[315]] is interposed between the first and second silicon oxide layers [[314,316]] ; and

(b.8) wherein the combination of the first and second silicon oxide layers and the first silicon nitride layer is interposed between the first and second silicon layers [[314,316]] .

11. The sidewall dielectric forming method [[300]] of Claim 10 and further wherein said plurality of exposed material layers of the ONO-type memory cell stack includes:

(b.9) a second silicon nitride layer [[319]]; disposed above the first silicon layer [[318]].

12. The sidewall dielectric forming method [[300]] of Claim 1 and further wherein:

a height variation ratio, $R_H = H_{outer}/H_{inner}$, determined for the ONO-type memory cell stack [[310"]] after formation of the sidewall dielectric by the dry ISSG process, is about 1.20 or less, where H_{inner} represents a stack height at a lateral position in the stack that is spaced away from the stack edges and where H_{outer} represents a stack height at a lateral position

near or at one of the stack edges.

13. The sidewall dielectric forming method [[300]] of Claim 1 and further wherein lateral sidewall breakdown voltages [[431,432]] are substantially uniform along the height of the ONO-type memory cell stack [[310"]] after formation of the sidewall dielectric by the dry ISSG process.

14. The sidewall dielectric forming method [[300]] of Claim 1 and further wherein a larger erase speed [[442]] is obtained in a memory cell having said ONO-type memory cell stack [[310"]] after formation of the sidewall dielectric by the dry ISSG process, where the larger erase speed [[442]] is larger than a corresponding erase speed [[441]] obtained in a corresponding memory cell having an ONO-type memory cell stack [[310"]] with sidewall dielectric formed by an HTO process [[120]] .

15. The sidewall dielectric forming method [[300]] of Claim 1 and further comprising:

(b) after said dry ISSG process, forming further and supplemental sidewall dielectric [[390]] by a non-ISSG sidewall dielectric forming process [[380]] .

16. A memory cell [[303]] having an ONO-type memory cell stack [[310]] where at least one sidewall of the ONO-type memory cell stack includes a plurality of material layers respectively composed of different materials, the memory cell [[303]] further comprising:

(a) a sidewall-coating dielectric [[350,390]] whose fabrication was at least initially started by subjecting at least one otherwise exposed and multi-layered sidewall of the ONO-type memory cell stack to a dry ISSG process (In-Situ Steam Generation).

17. The memory cell [[303]] of Claim 16 wherein the dry ISSG process used to fabricate the memory cell comprises:

(a.1) generating a sufficient amount of atomic oxygen [[325]] near said at least one otherwise exposed sidewall of the ONO-type memory cell stack so as to substantially oxidize exposed sidewall regions of those of the different materials of the ONO-type memory cell stack that are not substantially oxidized prior to said subjecting of the at least one otherwise exposed sidewall to said dry ISSG process.

18. The memory cell [[303]] of Claim 16 wherein the dry ISSG process used to fabricate the memory cell comprises:

(a.1) flowing molecular oxygen (O_2) towards the stack; and

(a.2) flowing molecular hydrogen (H_2) towards the stack, where the volumetric flow ratio of the H_2 to the O_2 is less than about 0.2.

19. A memory cell [[303]] having an ONO-type memory cell stack [[310]] isolated by sidewall dielectric [[350,390]] where at least one dielectric-isolated sidewall of the ONO-type memory cell stack includes a plurality of material layers respectively composed of different materials, the memory cell [[303]] being further characterized by :

(a) a height variation ratio, $R_H = H_{outer}/H_{inner}$, determined for the ONO-type memory cell stack [[310"]] after formation of the sidewall dielectric, where the height variation ratio, R_H is about 1.20 or less, where H_{inner} represents a stack height at a lateral position in the stack that is spaced away from the stack edges and where H_{outer} represents a stack height at a lateral position near or at one of the stack edges.

20. A memory cell [[303]] having an ONO-type memory cell stack [[310]] isolated by sidewall dielectric [[350,390]] where at least one dielectric-isolated sidewall of the ONO-type memory cell stack includes a plurality of material layers respectively composed of different materials, the memory cell [[303]] being further characterized by :

(a) lateral sidewall breakdown voltages [[431,432]] that are substantially uniform along the height of the ONO-type memory cell stack [[310"]] .